(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
16 May 2002 (16.05.2002)

PCT

(10) International Publication Number
WO 02/39607 A1

(51) International Patent Classification[7]: H04B 1/707

(21) International Application Number: PCT/GB01/04847

(22) International Filing Date:
1 November 2001 (01.11.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
0027540.4 10 November 2000 (10.11.2000) GB

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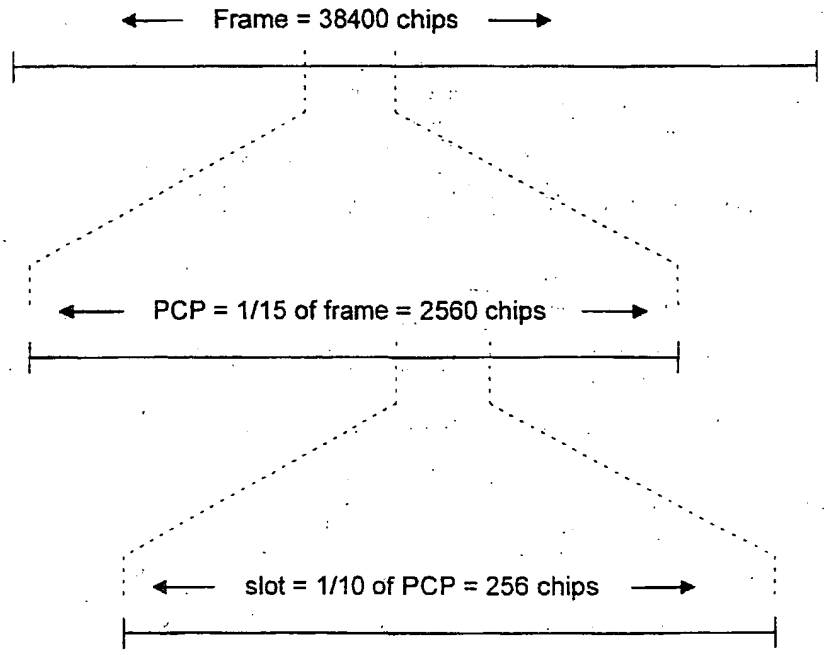
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

[Continued on next page]

(54) **Title:** TIME ALIGNMENT IN A CDMA SYSTEM



(57) **Abstract:** A receiver for efficiently synchronising itself with a signal having the frame structure shown in Figure (1). Each power control period (PCP) of the received signal contains a primary synchronisation sequence (PSCH) in one of its slots. The receiver correlates the known PSCH against the received signal to determine the position of the PSCH in the received signal and thereby synchonise itself with the received signal. To conserve processing resources, the correlation can be truncated where a sufficiently good correlation is achieved before the nominal end of the correlation routine.

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TIME ALIGNMENT IN A CDMA SYSTEM

The invention relates to methods and apparatus for time aligning a receiver with a received signal. In particular, the invention relates to determining the position of a known synchronisation marker or data-string in a received signal to facilitate the carrying out of other processes (such as frequency locking and data decoding) on the received signal.

The frame structure of a signal received by, for example, a mobile telephone, is shown in Figure 1. The received signal comprises a sequence of consecutive chips, each of a fixed duration. Each chip comprises a pair of I (in-phase) and Q (quadrature) values and in that sense each chip, r, is a complex number $r = r_x + j\, r_y$, where r_x and r_y represent, respectively, the I and Q values comprising the chip. Each of the IQ chip pairs can be thought of as a symbol. As shown in Figure 1, the frame structure comprises a frame 38400 chips long. The frame is constituted by 15 consecutive power control periods (PCP), each 2560 chips long. Each PCP comprises 10 consecutive slots, each 256 chips long. One of the slots (in each PCP) contains a synchronisation word (SW) which is 256 chips, or symbols, in length.

The apparatus receiving the signal of Figure 1, searches the received signal looking for the synchronisation word (SW) so that the receiver can time align itself with the received signal to achieve frequency locking and correct decoding of the received information.

Conventional methods of time-aligning a receiver with a received signal are time consuming and computationally intensive.

The present invention aims to ameliorate these problems.

According to one aspect, the invention provides a method of synchronising a receiver to a received signal comprising a series of chips arranged in successive periods, the method comprising correlating a synchronisation word with a number of period lengths of the received signal, accumulating the correlation results to produce first cumulative correlation results, and examining the first cumulative correlation results to determine the position of

The threshold used in the truncation may be predetermined or it may be determined dynamically.

In the synchronisation process, the receiver operates on a test section of the incoming signal which is at least one period length in duration. Preferably, the receiver operates on a section which is 3 to 8 period lengths in duration. Of course, the number of period-lengths used in the correlation process will be reduced where the truncation intercedes.

In a preferred embodiment, the receiver is a UMTS receiver and the synchronisation word is a primary synchronisation sequence, PSCH.

By way of example only, an embodiment of the invention will now be described with reference to the accompanying figure in which:

It will be apparent that a period length need not be synchronised with the periods of the received signal.

Figure 1 illustrates the frame structure of a received signal.

In this embodiment, the receiver operates on a signal having the frame structure discussed earlier with reference to Figure 1. The receiver performs the synchronisation process by operating on a test length of the received signal which is (according to default criteria) 6 PCPs long.

The receiver correlates the SW with the PCP length using the equation:

$$P_k = \left(\sum_{i=0}^{255} (s_i \cdot r_{x\,(i+k)})\right)^2 + \left(\sum_{i=0}^{255} (s_i \cdot r_{y\,(i+k)})\right)^2$$

It is possible to translate the chip boundaries in the test section by a one-half chip offset. The correlation process can then be repeated, calculating a power array for each PCP-length and building up another final power array. This new final power array will contain a maximum value indicating the initial chip of the SW in the received signal. The maximum values from the original final power array and the new final power array can be compared and the greater of the two be taken to indicate the position of the initial chip of the SW in the received signal. It will be appreciated that this is a way of increasing the resolution of the process of locating the SW in the received signal. Furthermore, it will be appreciated that the chip boundaries in the test section could be shifted by other fractions of a chip. In fact, a final power array could be calculated for each of any number of offsets (each offset being a different fraction of a chip) to increase the resolution further.

To expedite the determination of the SW position in the received signal, a truncation decision is used in the process of calculating a final power array. Prior to beginning the calculation of a P_k array for each of the second and subsequent PCP lengths (here, the 2nd to 6th PCP-lengths), the receiver checks the cumulative power array to determine if any of the k elements therein exceeds predetermined a threshold. If so, the cumulative power array becomes the final power array and no further PCP lengths are processed in the creation of that final power array.

Where plural final power arrays are created (on the basis of different chip-fraction offsets), it will be apparent that each final array must be based on the same number of accumulated power arrays P_k (or PCP-lengths). Otherwise, the final power arrays could not be compared on a fair basis for determining the position of the synchronisation word on the received signal. Hence, if a truncation of the number of PCP-lengths processed occurs in the creation of the first final power array, then the same truncation is applied in the creation of all the subsequent final power arrays (without recourse to threshold comparison).

7. A method according to claim 5 or 6, wherein the step of examining cumulative correlation results comprises locating a maximum correlation value in the cumulative correlation results.

8. A method according to claim 7, wherein, in the step of examining cumulative correlation results, a located maximum correlation value is deemed to indicate the beginning of the synchronisation word in the received signal.

9. A computer program for implementing the method of any one of the preceding claims.

10. Apparatus for synchronising a receiver to a received signal comprising a series of chips arranged in successive periods, the apparatus comprising correlating means for correlating a synchronisation word with a number of period-lengths of the received signal, accumulating means for accumulating the correlation results to produce first cumulative correlation results, and examining means for examining the first cumulative correlation results to determine the position of the synchronisation word in the received signal, wherein the apparatus further comprises truncating means for truncating said number where the first cumulative correlation results exceed a threshold.

11. Apparatus according to claim 10, further comprising displacing means for displacing the beginnings of the period-lengths to produce shifted lengths and conforming means, wherein the correlating means is arranged to correlate the synchronisation word with a number of shifted lengths to produce second cumulative correlation results, the examining means is arranged to examine the second cumulative correlation results to determine the position of the synchronisation word in the received signal and the conforming means is arranged to conform the said number of shifted lengths to the number of lengths used to generate the first cumulative correlation results.

12. Apparatus according to claim 11, wherein the displacing means is arranged to displace the beginnings of the period-lengths by a fraction of a chip.

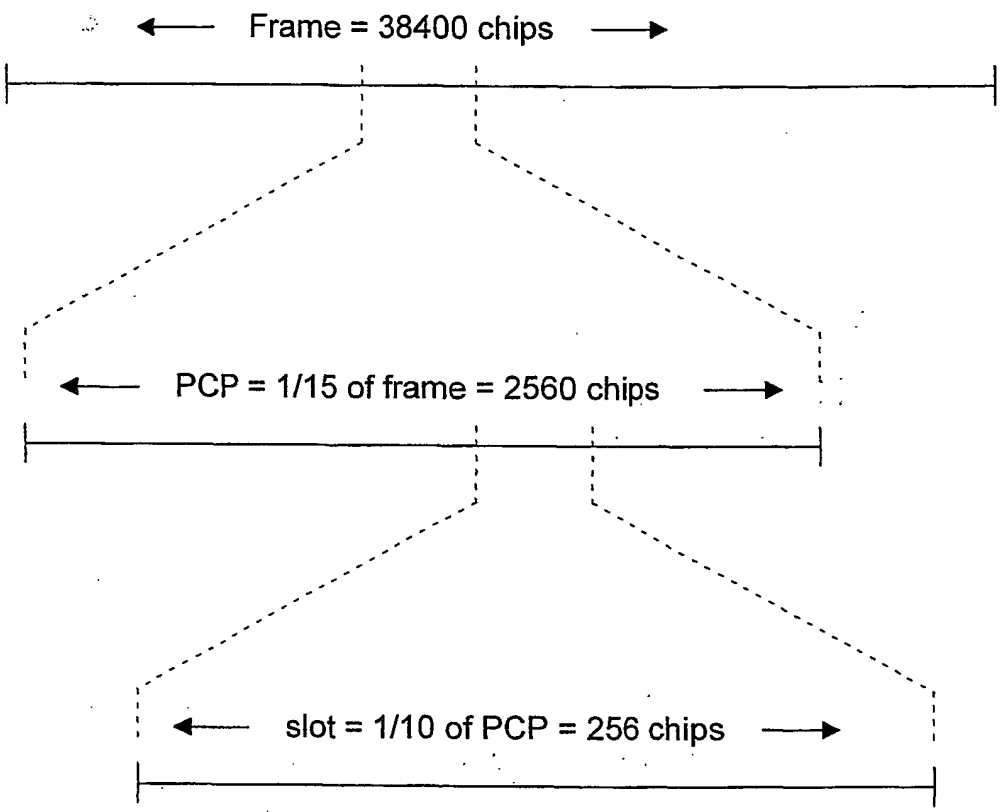

Figure 1

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